PERMANENT MEMORANDUM NO. M-1113

SUBJECT: Programmed Data Processor Specifications
DATE: June 27, 1961
TO: PDP Distribution List
FROM: John Koudela

A. Central Processor

1. Programming and Numerical System

a. Binary internal number system

b. Fixed word length of 18-bits, including sign

c. One instruction per word

d. Fixed point arithmetic

e. Single address

f. Multiple-step indirect addressing

g. Number of instructions (see complete instruction list for PDP-1)

(1) 29 basic, including 1 input-output

(2) 57 total, excluding input-output

(3) 43 specified input-output

(4) 100 total, including all input-output

2. Arithmetic Unit

a. Addition time: 10 microseconds, including all access.

b. Subtraction time: 10 microseconds, including all access.

c. Multiplication time: by subroutine, 325 microseconds average; automatic, 25 microseconds maximum.

d. Division time: by subroutine, 440 microseconds average; automatic, 40 microseconds maximum.

3. Instruction Execution Times (except arithmetic)

   a. All instructions require either 5 or 10 microseconds for completion.

   b. Each step of indirect addressing requires an additional 5 microseconds.

   c. Input-output instructions require 5 microseconds in asynchronous operations, whereas in synchronous operations, the time depends upon the input-output device being used.

   d. The "Execute" instruction requires 5 microseconds plus the time of the instruction executed.

   e. Combined Skip instructions and combined Operate instructions require 5 microseconds.

4. Internal operation of the PDP-1 is parallel, synchronous, and sequential. Input-output is basically synchronous and sequential. Asynchronous and/or concurrent operations of input-output devices can be approached with proper programming techniques, or truly performed with input-output devices connected through high speed input-output channels.

5. Storage Unit

   a. Random access, coincident-current, magnetic core (non-volatile).

   b. Number of words: 4,096 to 32,768 in increments (modules) of 4,096.

   c. Number of binary per word: 18

   d. Equivalent number of decimal digits per word: 5 +

   e. Equivalent number of alphanumeric characters per word: 3

   f. Number of instructions per word: 1

   g. Storage access time: 5 microseconds

B. Input-Output

1. Magnetic Tape

a. Naximum number of units: 24

b. Number of characters per inch: 200

c. Number of bits per character (6 binary or alphanumeric and 1 parity): 7

d. Inter-record (inches): 3/4

e. Tape speed (inches per second): 75

f. Transfer rate (characters per second): 15,000

g. Start-stop time (milliseconds): 3

h. Width of tape (inches): 1/2

i. Length of reel (feet): 2400

j. Variable tape format, including standard I.B.M.

The Basic Tape Control Unit transfers information one character at a time under program control. Read, write, and compute operations are performed sequentially.

The High Speed Tape Control Unit automatically transfers information in blocks of characters. Compute and read or write operations can be performed concurrently. Special features include scatter-read and gather-write; automatic, bit-by-bit read-compare with core memory; automatic sorting functions.

2. Punched tape

a. Number of line per inch: 10

b. Number of channels per line: 5, 6, 7, or 8 (8 is standard).

c. Read speed (lines per second): 400

d. Punch speed (lines per second): 63

e. Reader is photoelectric and starts and stops on a line.

f. Character listing is alphanumeric plus special characters.

g. Compute and read or punch operations can be performed concurrently through the use of the Sequence Break System, or can be approached through proper programming.

3. Typewriter

a. 10 characters per second output.

b. Character listing is alphanumeric plus special characters.

c. Compute and input or output operations can be performed concurrently as with punched tape.

4. Line Printer

a. Lines per minute: 450

b. Columns per line: 72

c. Character listing is alphanumeric plus special characters.

d. Compute and print operations can be performed concurrently as with punched tape.

C. Special Equipment

1. Sequence Break System. Allows concurrent operation of several input-output devices and the main sequence. The standard PDP-1 is equipped with a one-channel sequence break whereas the 16-channel sequence break system is optional.

2. Cathode Ray Tube Display and Light Pen. Displays information at a rate of 20,000 points per second. Light Pen allows for the "Input" of information. The Visual 16" CRT Display has a resolution of 1 part in 1,024, whereas the Precision 5" CRT Display has a resolution of 1 part in 4,096.

3. Eighteen-bit Real Time Clock. Provides real time synchronization to the Central Processor. The clock is an 18-bit

binary counter controlled by a crystal oscillator.

4. Punched Card Input-Output Control. Allows on-line operation of standard, 80 column card, input-output equipment. The control is for use with the I.B.M. 523 Summary Punch for both input and output at speeds of 100 cards per minute.

5. High Speed Input-Output Channels. Allows for high speed, concurrent operation of several input-output devices and the main sequence. The standard PDP-1 has provisions to add 3 high speed channels.

6. Input-Output Instruction Control Panel. Allows for simple addition of special input-output transfer instructions as required.

7. Basic Spare Parts Package. Provides one or two spare plug-in modules for each module-type used in the Central Processor.

D. Checking Features

1. Accumulator Overflow

2. Lateral Parity check on Magnetic tape

   a. While reading using basic control.

   b. While both reading and writing using high speed control.

3. Magnetic Tape Read-Compare instruction to compare data on tape with data in storage, bit by bit.

4. Built in Marginal Checking Facilities for all sub-assemblies in the Central Computer.

E. Power, Space, Weight, and Site Preparation

1. Power requirements, 115 volts, 60 cycles per second, single phase, 1500 watts.

2. Standard PDP-1 weight: 1500 pounds.

3. Standard PDP-1 dimensions, 98.5 inches wide, 24.5 inches deep, and 69.5 inches high.

4. Ambient room temperature and relative humidity

   a. 50 to 110 degrees Fahrenheit

   b. 20 to 70 percent relative humidity

5. Site preparation not required

F. Production Record

1. Time required for delivery, 6 to 9 months from date of order.

2. Number of systems produced, over 5 (6-61)

G. Services

1. Basic program and subroutine library supplied with each PDP-1:

   a. FRAP, The PDP-1 Assembly Program for fixed or floating point arithmetic.

   b. DECAL, The PDP-1 Compiler Program for fixed or floating point arithmetic.

   c. Single Precision Floating Point Package for arithmetic using an 18-bit fraction and an 18-bit exponent. The package includes all standard function generator subroutines.

   d. Double Precision Floating Point Package for arithmetic using a 36-bit fraction and an 18-bit exponent. The package includes all standard function generator subroutines.

   e. Basic Double Precision Fixed Point subroutines, including addition, subtraction, multiplication and division.

   f. All standard function generator subroutines for single precision fixed point.

   g. Utility Routine Package, including input-output subroutines and debugging aids.

2. Programming, operating, and maintenance training and materials are provided by the manufacturer.

3. Membership in the active PDP-1 User's Society is available.

Definition of a Standard PDP-1 Computer System

A. Standard PDP-1 consists of:

1. Central Processor (with 4,096, 18-bit word core memory).

2. Control Console.

3. Punched Tape Reader (photoelectric), read speed 400 lines per second.

4. Punched Tape Punch, punch speed 63 lines per second.

5. Alphanumeric Typewriter (with 18-inch, pin-feed platen).

6. One Channel Sequence Break System.

7. Input-Output Instruction Control Panel.

8. Programmed multiply and divide using Multiply Step and Divide Step instructions.

9. Total number of instructions: 64.

Complete Instruction List for PDP-1

Y means the contents of memory location Y

N means number

AC means accumulator

IO means input-output register

PC means program counter

TW test word switches

A. Basic Instructions, including one input-output

	Instruction	Code	Time(us)	Definition
1.	ADD Y	40	10	Add to AC
2.	SUB Y	42	10	Subtract from AC
3.	MUS Y	54	10	Multiply step using Multiplier Y
4.	DIS Y	56	10	Divide step using divisor Y
5.	IDX Y	44	10	Index Y
6.	ISP Y	46	10	Index Y and skip if positive AC
7.	AND Y	02	10	Logical and with Y
8.	XOR Y	06	10	Exclusive or with Y
9.	IOR Y	04	10	Inclusive or with Y
10.	LAC Y	20	10	Load AC with Y
11.	DAC Y	24	10	Deposit AC in Y
12.	DAP Y	26	10	Deposit address part in Y
13.	DIP Y	30	10	Deposit instruction part in Y
14.	LIO Y	22	10	Load IO with Y
15.	DIO Y	32	10	Deposit IO in Y
16.	DZM Y	34	10	Deposit zero in memory Y
17.	XCT Y	10	5 +	Execute instruction in Y
18.	JMP Y	60	5	Jump to Y

Instruction	Code	Time(us)	Definition
19. JSP Y	62	5	Save PC in AC and jump to Y
20. CAL	16	10	Call subroutine
21. JDA Y	17	10	Deposit AC in Y and JSP Y + 1
22. SAD Y	50	10	Skip if AC different than Y
23. SAS Y	52	10	Skip if AC same as Y
24. LAW N	70	5	Load AC with N
25. SFT N	66	5	Shift-rotate group
26. SKP	64	5	Skip group
27. OPR	76	5	Operate group
28. IOT	72		Input-output transfer group
29. JFD Y	12	10	Jump field according to Y (field switching for expanded memories)
B. Micro-Instructions, Except Input-output			
30. LAW -N	71	5	Load AC with -N
Shift-rotate Group			
31. RAR N	671	5	Rotate AC right N places
32. RAL N	661	5	Rotate AC left N places
33. SAR N	675	5	Shift AC right N places
34. SAL N	665	5	Shift AC left N places
35. RIR N	672	5	Rotate IO right N places
36. RIL N	662	5	Rotate IO left N places
37. SIR N	676	5	Shift IO right N places

	Instruction	Code	Time(us)	Definition
38.	SIL N	666	5	Shift IO left N places
39.	RCR N	673	5	Rotate combined AC-IO right N places
40.	RCL N	663	5	Rotate combined AC-IO left N places
41.	SCR N	677	5	Shift combined AC-IO right N places
42.	SCL N	667	5	Shift combined AC-IO left N places
Skip Group				
43.	SZA	64 0100	5	Skip on zero AC
44.	SNA	65 0100	5	Skip on non-zero AC
45.	SPA	64 0200	5	Skip on positive AC
46.	SMA	64 0400	5	Skip on minus AC
47.	SZO	64 1000	5	Skip on zero overflow
48.	SNO	65 1000	5	Skip on non-zero overflow
49.	SPI	64 2000	5	Skip on positive IO
50.	SMI	65 2000	5	Skip on minus IO
51.	SZS N	64 00s0	5	Skip on zero sense switch N
52.	SNS N	65 00s0	5	Skip on non-zero sense switch N
53.	SZF N	64 000F	5	Skip on zero flag N
54.	SNF N	65 000F	5	Skip on non-zero flag N

Instruction	Code	Time(us)	Definition
Operate Group			
55. CLI	76 4000	5	Clear IO
56. LAT	76 2000	5	Load AC from TW
57. CMA	76 1000	5	Complement AC
58. HLT	76 0400	5	Halt
59. CLA	76 0200	5	Clear AC
60. CLF N	76 000F	5	Clear flag N
61. STF N	76 001F	5	Set flag N
C. Specified Input-Output Instructions (Micro IOT Instructions)			
Reader			
62. RPA	IOT 01		Read punched tape, Alphanumeric
63. RPB	IOT 02		Read punched tape, Bi-octal
64. RRB	IOT 30		Read reader buffer (for sequence break operations)
Punch			
65. PPA	IOT 05		Punch punched tape, Alphanumeric
66. PPB	IOT 06		Punch punched tape, Bi-octal
Typewriter			
67. TYO	IOT 03		Type out
68. TYI	IOT 04		Type in

Instruction	Code	Time(us)	Definition
Display			
69. DPY	IOT 07		Display one point on CRT
Card Reader			
70. RAC	IOT 41		Read a card
71. RSC	IOT 42		Row synchronize and clear field counter
72. RAF	IOT 32		Read a field of 18 columns and index field counter
73. CKS	IOT 33		Check status of reader
Card Punch			
74. PAC	IOT 43		Punch a card
75. PSC	IOT 44		Row synchronize and prepare to punch first field
76. PAG	IOT 22		Punch a field of 18 columns
Basic Magnetic Tape			
77. MCB	IOT 70		Magnetic tape clear buffer
78. MWC	IOT 71		Magnetic tape write character
79. MRC	IOT 72		Magnetic tape read character
80. MCS	IOT 34		Magnetic tape check status
81. MSM	IOT 73		Magnetic tape select mode
High Speed Magnetic Tape			
82. MUF	IOT 75		Magnetic tape unit and final address
83. MIC	IOT 76		Magnetic tape initial address and command

Instruction	Code	Time(us)	Definition
84. MEL	IOT 35		Magnetic tape examine location
85. MES	IOT 36		Magnetic tape examine status
86. MRI	IOT 66		Magnetic tape reset initial address
87. MRF	IOT 67		Magnetic tape reset final address
Clock			
88. RSK	IOT 47		Reset the clock
89. RDK	IOT 37		Read clock time into IO
Timer			
90. STM	IOT 24		Set timer with IO
Relay Buffer			
91. SRB	IOT 21		Set Relay Buffer
Analog to Digital Converter			
92. CNV	IOT 41		Convert a voltage
93. RCB	IOT 31		Read converter buffer
Sequence Break System			
94. ESM	IOT 55		Enter sequence break mode
95. LSM	IOT 54		Leave sequence break mode
96. ASC	IOT 51		Activate selected sequence break channel
97. DSC	IOT 50		Deactivate selected sequence break channel

Instruction	Code	Time(us)	Definition
98. ISB	IOT 52		Initiate sequence break to selected channel
Drum System			
99. DRT	IOT 61		Drum transfer
100. DRA	IOT 62		Current drum address to IO
101. DBA	IOT 63		Drum block address (for sequence break operations)
Core Memory Expansion			
102. CFD	IOT 74		Change fields
103. CDF	IOT 74		Change data field
Line Printer			
104. PRT	IOT 45		Print
105. PRL	IOT 46		Print load buffer from IO
106. PAP	IOT 23		Print advance paper

D. Optional Instructions

104. MUL Y	54	25	Multiply by Y (replaces multiply step)
105. DIV Y	56	40	Divide by Y (replaces divide step)

E. Instruction List Summary

1. Number of Basic Instructions: 25
   (SFT, SKP, OPR, IOT are omitted since they each represent a micro-instruction group)

2. Number of Micro-instructions: 32
   (except IOT)

3. Specified IOT instructions: 45

4. Total number of available instructions: 102